METHODS AND SYSTEMS FOR TIMING-DRIVEN CIRCUIT SYNTHESIS

Abstract of the Disclosure

Aspects of the present invention include a methodology for the general timing-driven iterative refinement-based approach, a timing-driven optimization (TDO) method that optimizes the circuit depth after the area oriented logic optimization, and a layout-driven synthesis flow that integrates performance-driven technology mapping and clustering with TDO to account for the effect of mapping and clustering during the timing optimization procedure of TDO. The delay reduction process recursively reduces the delay of critical fanins of a selected. Furthermore, in one embodiment, the fanins of the selected node are sorted according to their slack values.